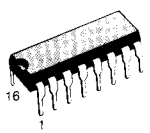
T54LS166
T74LS166

8-BIT SHIFT REGISTER

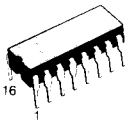
DESCRIPTION

The T54LS/T74LS166 is an 8-bit shift register. It consists of a parallel-in or serial-in, serial-out 8 bit shift register with gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/LOAD input. When the SHIFT/LOAD input is held high, the serial data input is enabled and the eight flip-flop perform serial shifting with each clock pulse. When held LOW, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high level edge of the clock pulse via a two input positive NOR gate. Clocking is inhibited when either of the clock inputs are held high, holding either input low enables the other clock inputs this will allow the system clock to be free running and the register stopped on command with the other clock inputs. The clock inhibit input should be changed to the high level only when the clock input is held high. A buffered direct input overrides all other inputs, including the clock, and sets all flip-flops to zero.

- DIRECT OVERRIDING CLEAR
- PARALLEL CONVERSION
- SYNCHRONOUS LOAD



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

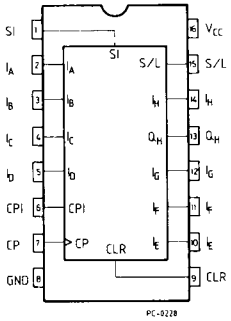
C1
Plastic Chip Carrier

ORDERING NUMBERS:

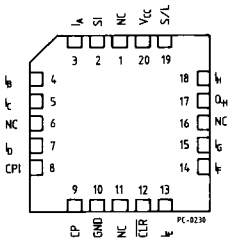
T54LS166 D2
T74LS166 D1
T74LS166 B1
T74LS166 C1
T74LS166 M1

PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

PIN NAMES

A,B,C,D, E,F,G,H	Parallel Inputs
CLR	Clear
SIL	Shift Load
Q_H	Outputs
SI	Serial Input
CP	Clock Pulse
CPI	Clock Inhibit

TRUTH TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

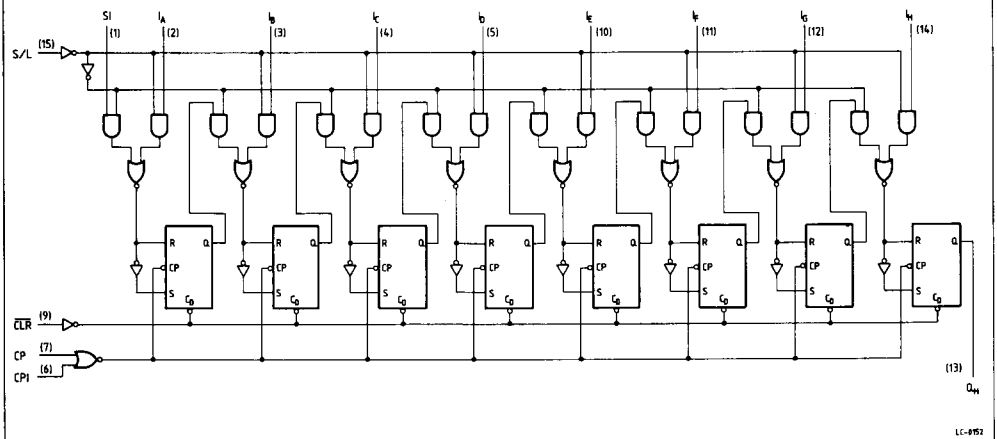
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS166D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS166XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

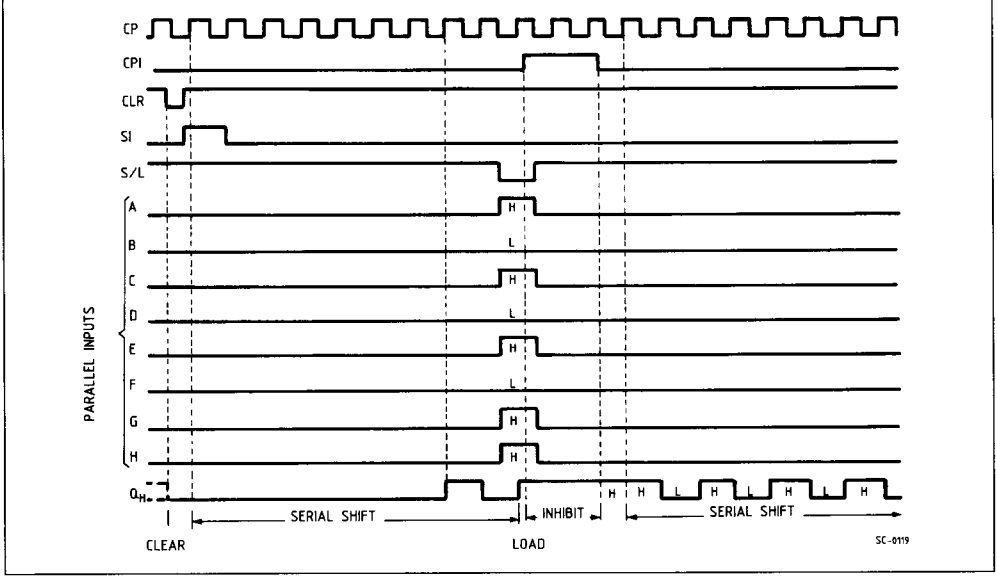
XX = package type.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

TYPICAL CLEAR, SHIFT, LOAD, INHIBIT, AND SHIFT SEQUENCES



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)	Units
			Min.	Typ.	Max.		
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA	
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V	μA mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX	mA
I_{CC}	Power Supply Current				38	V_{CC} = MAX	mA

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	25	35		V_{CC} = 5.0V C_L = 15pF	MHz
t_{PHL}	Clear to Output		19	30		ns
t_{PLH} t_{PHL}	Clock to Output		23 24	35 35		ns

Notes:
1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

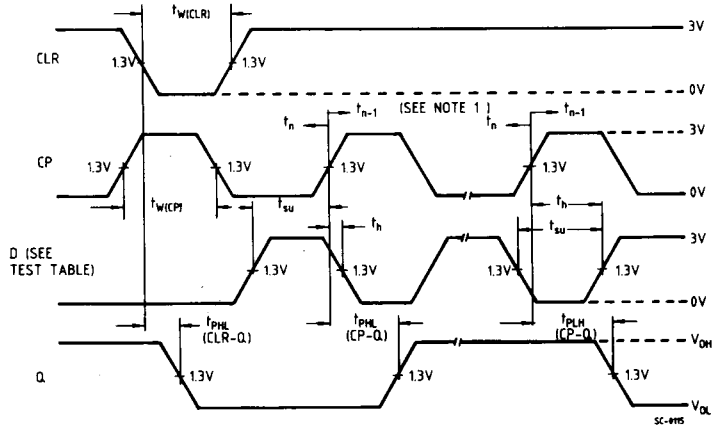
AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_W	Clock Clear Pulse Width	30			$V_{CC} = 5.0V$	ns
t_s	Mode Control Set-up Time	30				ns
t_s	Data Set-up Time	20				ns
t_h	Hold Time, Any Input	15				ns

AC WAVEFORMS

TEST TABLE FOR SYNCHRONOUS INPUT

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED
H	0V	O_H at t_{n+1}
Serial Input	4.5V	O_H at t_{n+8}



Note: t_n = bit time before clocking transition
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after eight clocking transitions